Amendments to the Claims:

1-21. (Cancelled)

22. (New) A semiconductor package comprising:

a die paddle having an opening formed therein;

at least two leads, one of the leads being disposed in spaced relation to the die paddle, with the remaining one of the leads being attached to the die paddle;

at least one semiconductor die having a source terminal electrically connected to the die paddle, a gate terminal electrically connected to the at least one of the leads disposed in spaced relation to the die paddle, and a drain terminal; and

a package body at least partially encapsulating the die paddle, the leads, and the semiconductor die such that portions of the leads and the drain terminal of the semiconductor die are exposed in the package body.

23. (New) The semiconductor package of Claim 22 wherein:

the die paddle defines opposed top and bottom surfaces; and

the source terminal of the semiconductor die is electrically connected to the bottom surface of the die paddle such that the gate terminal is aligned with and exposed in the opening.

24. (New) The semiconductor package of Claim 23 wherein the at least one lead disposed in spaced relation to the die paddle is electrically connected to the gate terminal of the semiconductor die via a conductive wire which is encapsulated by the package body.

25. (New) The semiconductor package of Claim 23 wherein:

the package body defines a bottom surface and a side surface;

the leads each define opposed top and bottom surfaces;

the drain terminal of the semiconductor die is exposed in the bottom surface of the package body;

a portion of each of the leads protrudes from the side surface of the package body.

26. (New) The semiconductor package of Claim 25 wherein:

the die paddle has a generally quadrangular configuration defining an opposed pair of peripheral edge segments; and

a plurality of the leads are included in the semiconductor package and segregated into two sets which are disposed along respective ones of the opposed peripheral edge segments of the die paddle.

27. (New) The semiconductor package of Claim 26 wherein at least one of the leads of each of the sets is attached to the die paddle.

28. (New) The semiconductor package of Claim 25 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads are disposed along a common one of the peripheral edge segments of the die paddle.

29. (New) The semiconductor package of Claim 23 wherein:

the package body defines a bottom surface;

each of the leads defines opposed top and bottom surfaces;

the drain terminal of the semiconductor die is exposed in the bottom surface of the package body; and

at least a portion of the bottom surface of each of the leads is exposed in the bottom surface of the package body.

30. (New) The semiconductor package of Claim 29 wherein:

the die paddle has a generally quadrangular configuration defining an opposed pair of peripheral edge segments; and

a plurality of the leads are included in the semiconductor package and segregated into two sets which are disposed along respective ones of the opposed peripheral edge segments of the die paddle.

31. (New) The semiconductor package of Claim 30 wherein at least one of the leads of each of the sets is disposed in spaced relation to the die paddle.

32. (New) The semiconductor package of Claim 29 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads are disposed along a common one of the peripheral edge segments of the die paddle.

33. (New) The semiconductor package of Claim 29 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

a plurality of the leads are included in the semiconductor package and disposed along each of the peripheral edge segments of the die paddle.

34. (New) The semiconductor package of Claim 29 wherein each of the leads includes a half-etched portion which is encapsulated by the package body.

35. (New) The semiconductor package of Claim 23 wherein:

the package body defines opposed top and bottom surfaces;

the drain terminal of the semiconductor die is exposed in the bottom surface of the package body; and

the top surface of the die paddle is exposed in the top surface of the package body.

36. (New) The semiconductor package of Claim 23 wherein:

the die paddle has a generally quadrangular configuration defining at least four corner regions; and

the opening comprises a notch formed in one of the four corner regions of the die paddle.

37. (New) The semiconductor package of Claim 23 wherein the opening comprises an aperture disposed in the die paddle.

38. (New) The semiconductor package of Claim 22 wherein the die paddle is sized and configured relative to the semiconductor die such that the gate terminal of the semiconductor die is not covered by the die paddle and thus exposed when the source terminal is electrically connected to the die paddle.

39. (New) A semiconductor package comprising:

a die paddle having an opening formed therein;

at least two leads, one of the leads being disposed in spaced relation to the die paddle, with the remaining one of the leads being attached to the die paddle;

a semiconductor die having a source terminal electrically connected to the die paddle, a gate terminal electrically connected to the at least one of the leads disposed in spaced relation to the die paddle, and a drain terminal; and

a layer of encapsulant partially encapsulating the die paddle, the leads, and the semiconductor die.

40. (New) The semiconductor package of Claim 39 wherein:

the die paddle defines opposed top and bottom surfaces; and

the source terminal of the semiconductor die is electrically connected to the bottom surface of the die paddle such that the gate terminal is aligned with and exposed in the opening.

41. (New) The semiconductor package of Claim 40 wherein the at least one lead disposed in spaced relation to the die paddle is electrically connected to the gate terminal of the semiconductor die via a conductive wire which is encapsulated by the layer of encapsulant.

42. (New) The semiconductor package of Claim 40 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads are disposed along a common one of the peripheral edge segments of the die paddle.

43. (New) The semiconductor package of Claim 22, further comprising:

a second die paddle having an opening formed therein;

at least two second leads, one of the second leads being disposed in spaced relation to the second die paddle, with the remaining one of the second leads being attached to the second die paddle; and

a second semiconductor die having a source terminal electrically connected to the second die paddle, a gate terminal electrically connected to the at least one of the second leads disposed in spaced relation to the second die paddle, and a drain terminal;

the package body further at least partially encapsulating the second die paddle, the second leads, and the second semiconductor die such that portions of the second leads and the drain terminal of the second semiconductor die are exposed in the package body.